

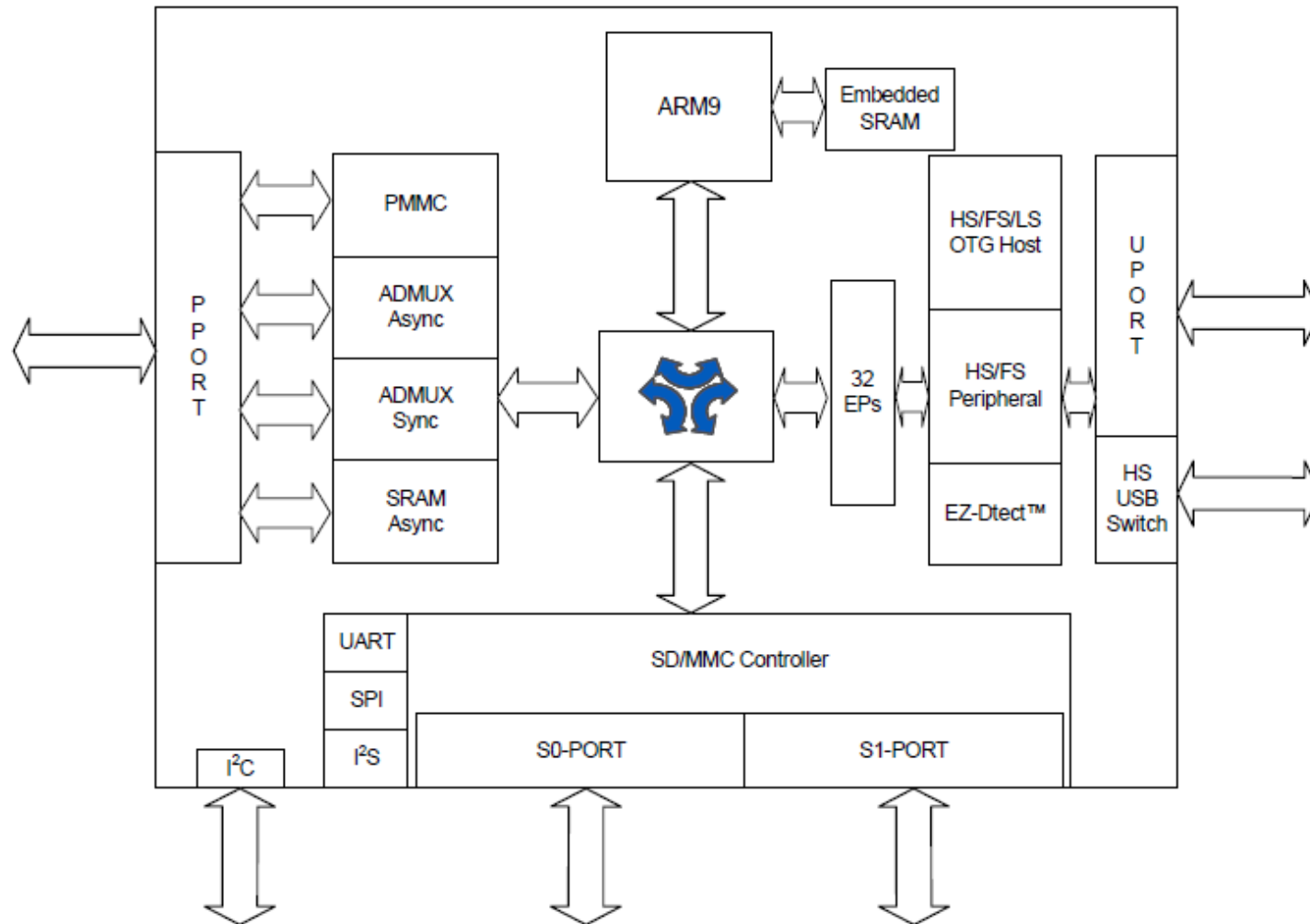
Testing a Complex USB3.0 SOC Device

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Outline

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- Device Overview
 - Data Sheet Parameters
 - IP Block Table
 - Test Chips
 - RTL Validation Before Silicon
 - Test Vector Debug Prior to Silicon
 - Device Bring up
 - Device Characterization
 - USB3.0 Compliance Testing
 - Production Test

Device Overview



- 4 Major Interface Ports
- 10 Power Supplies
- 73 Clocks
- 225 Timing Parameters
- 24 IP Blocks
- Multiple Embedded SRAMs

- Power Supply Voltages
- I_{dd}
- DC Levels
- Timing Parameters

- Power Supplies

- Core
- Efuse
- USB3.0
- PPort IO, SPort IO
- VBUS/VBATT

- Power Modes

- Operating
- 4 Standby

- IO Pins

- Leakage
- Vil/Vih
- Vol/Voh

Interface Timing Parameters (1)

- Host Processor Interface (P Port)
 - Async SRAM
 - ADMux Memory
 - Sync ADMux Memory
 - PMMC
 - GPIF
- Storage Port (S PORT)
 - MMC V4.4
 - MMC20, MMC26, MMC-HS, MMCDDR52
 - SD V3.0
 - SD-SRD12, SD-SDR25, SD-SDR50, SD-DDR50

Interface Timing Parameters (2)

- USB Port (U PORT)
 - USB3.0 Super Speed, 5.0Gb/s
 - USB2.0 Full/High Speed, 12Mb/s, 480Mb/s
 - USB Switch
- Low Performance Peripherals (LPP)
 - I2C, 100kHz, 400kHz, 1MHz
 - I2S, 32kHz, 44.1kHz, 48kHz
 - SPI, 33MHz
 - UART

IP Block Table

-
- | | |
|--------------------------|---------|
| • USB3 Phy | • Efuse |
| • USB2 Phy | • ESD |
| • USB2 Switch | • SIB |
| • ACA | • UIB |
| • Temp Sensor | • PIB |
| • Body Bias
Generator | • SRAM |
| • ARM 9 CPU | • ROM |
| • Bandgap | • I2C |
| • Regulators | • I2S |
| • Output Voltage
Hold | • UART |
| • PLL | • SPI |
| • DLL | |
| • Crystal | |

UMC LL65 Test Chips

- Series 1
 - ESD
 - E-test
 - SRAMs
- Series 2
 - IOs
 - PLL
 - Regulators
- Series 3
 - USB2.0
 - USB3.0
 - Floor Plan For Noise Generation
- Series 4
 - Not done
 - Register Map

RTL Validation Prior to Silicon



Test Vector Debug Prior to Silicon

- Pattern Types
 - Scan
 - RAM BIST
 - Timing Characterization
 - IP Block Access
- Tools
 - Verilog Development
 - Functional Replay
 - Timing Replay
 - Internal Node Waveform Viewer

Device Bring Up

- Bench Functionality
- V93k
- Nextest
- USB3.0 Compliance

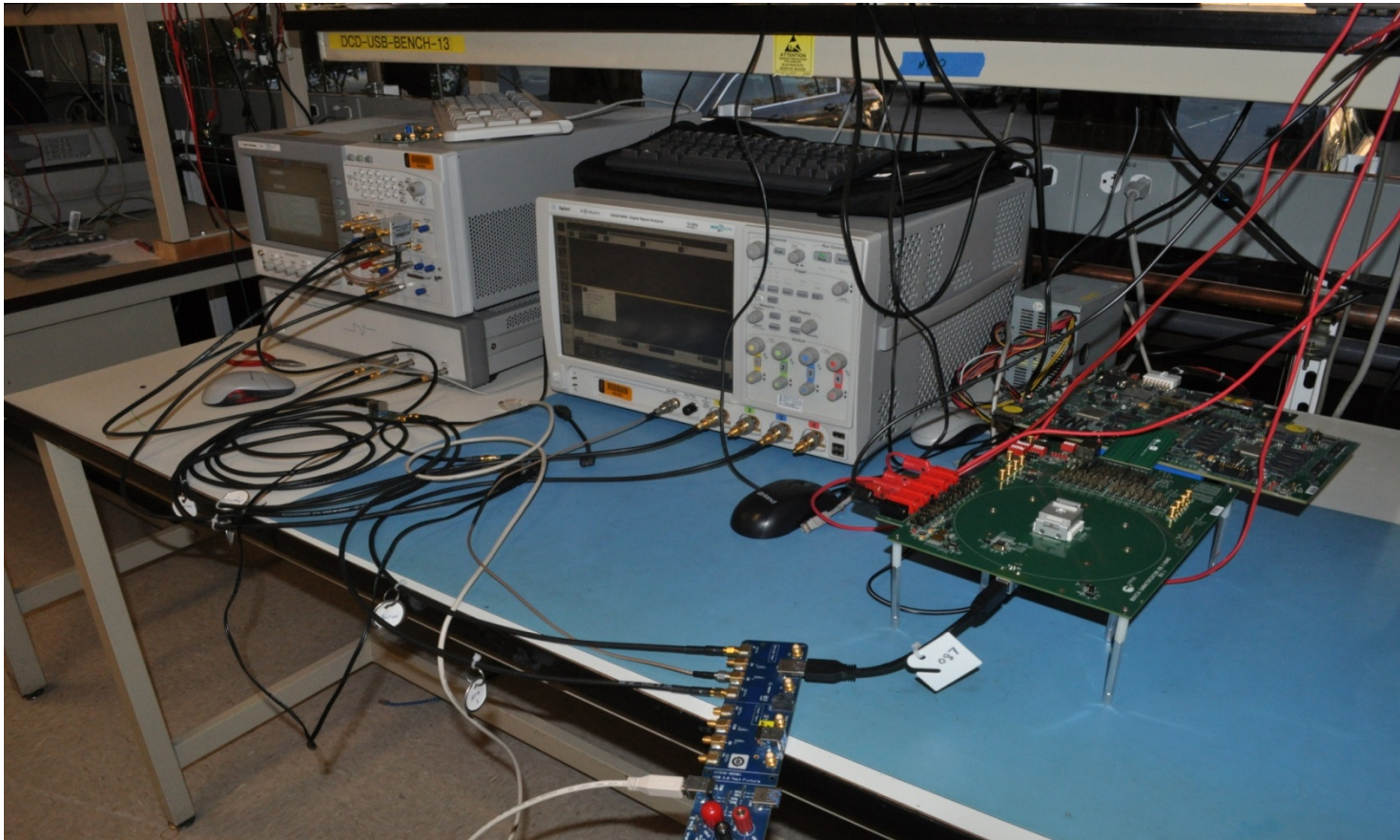
Are All the Voltages Correct?



Device Characterization

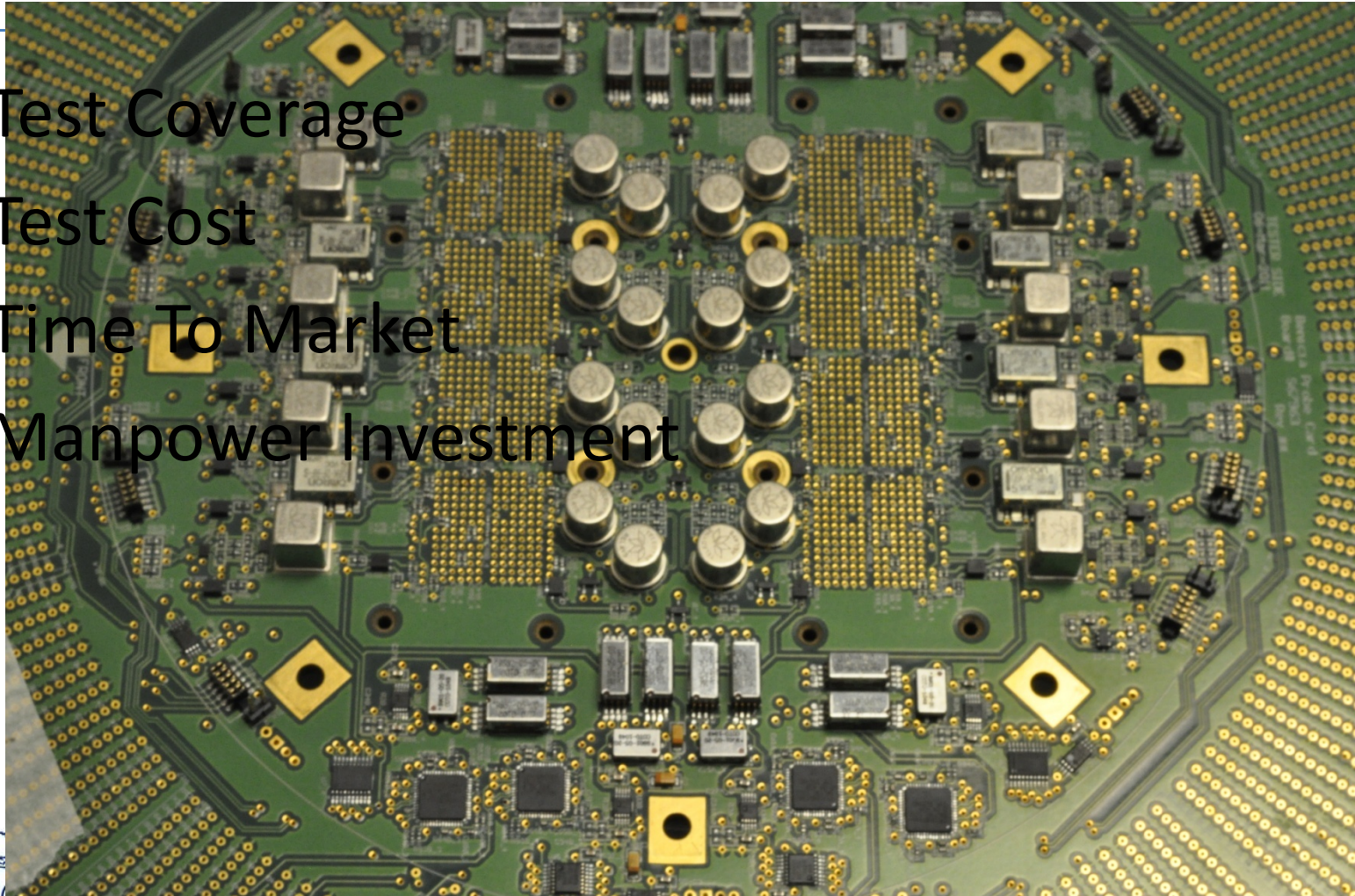
- All Data Sheet Parameters
- DC Parameters on Nextest or V93k
- AC Parameters on V93k

USB3.0 Compliance



Production Test

- Test Coverage
- Test Cost
- Time To Market
- Manpower Investment



Trade Offs

- Test Coverage
- Test Cost
- Time To Market
- Manpower Investment